CLAIMS

What is claimed is:

1. A method for performing conditional reads of a retirement payload array in a microprocessor, said method comprising:

receiving a clock signal, said clock signal having a first or "A" phase and a second or "B" phase;

receiving an advance pointer signal, said advance pointer signal having a first or inactive phase and a second or active phase, said second or active phase of said advance pointer signal corresponding to a shift in position of a read pointer of said retirement payload array;

initiating a read of said retirement payload array only when, both:

said clock signal is in said "B" phase;

and said advance pointer signal is in said active phase.

2. The method of Claim 1, wherein;

said retirement payload array comprises M rows of memory cells and N columns of memory cells.

3. The method of Claim 2, wherein;

said retirement payload array comprises M read word lines and N read bit lines, further wherein;

each of said N read bit lines is coupled to a corresponding pre-charge device and a corresponding sensing device.

4. The method of Claim 3, wherein

said pre-charge devices are pre-charged when said clock signal is in said first or "A" phase.

5. The method of Claim 4, wherein;

each of said pre-charge devices is a transistor and each of said sensing devices is a latch.

6. The method of Claim 5, wherein;

said number of rows M is equal to 16 and said number of columns N is equal to 192 such that said retirement payload array is a 192 column and 16 row retirement payload array.

7. The method of Claim 5, wherein;

said retirement payload array is a 192 column, 16-read word line register file structure employing a dynamic, full swing pull down read mechanism.

8. A method for performing conditional reads of a retirement payload array in a microprocessor, said method comprising:

providing a retirement payload array, said retirement payload array comprising M rows of memory cells and N columns of memory cells; said retirement payload array further comprising M read word lines and N read bit lines, wherein, each of said N read bit lines is coupled to a corresponding pre-charge device and a corresponding sensing device;

coupling a clock signal to said retirement payload array, said clock signal having a first or "A" phase and a second or "B" phase; wherein said pre-charge devices are pre-charged when said clock signal is in said first or "A" phase;

coupling an advance pointer signal to said retirement payload array, said advance pointer signal having a first or inactive phase and a second or active phase, said second or active phase of said advance pointer signal corresponding to a shift in position of a read pointer of said retirement payload array;

initiating a read of said retirement payload array only when, both:

said clock signal is in said "B" phase; and

said advance pointer signal is in said active phase.

9. The method of Claim 8, wherein;

said number of rows M is equal to 16 and said number of columns N is equal to 192 such that said retirement payload array is a 192 column and 16 row retirement payload array.

10. The method of Claim 8, wherein;

said retirement payload array is a 192 column, 16-read word line register file structure employing a dynamic, full swing pull down read mechanism.

11. A retirement payload array comprised of modified column structures, each of said modified column structures comprising:

a read bit line;

a pre-charge device coupled to said read bit line;

a sensing device coupled to said read bit line;

at least one memory cell, said memory cell comprising an output coupled to said read bit line and an input;

a gate, said gate comprising an output coupled to said input of said at least one memory cell and an input;

a conditional read circuit, said conditional read circuit comprising a first input, a second input and an

output, said conditional read circuit output being coupled to said input of said gate,

a clock signal, said clock signal having a first or "A" phase and a second or "B" phase, said clock signal being coupled to said second input of said conditional read circuit;

an advance pointer signal, said advance pointer signal having a first or inactive phase and a second or active phase, said second or active phase of said advance pointer signal corresponding to a shift in position of a read pointer, said advance pointer signal being coupled to said first input of said conditional read circuit, wherein;

said conditional read circuit initiates a read of said retirement payload array only when, both:

said clock signal is in said "B" phase; and

said advance pointer signal is in said active phase.

12. The retirement payload array of Claim 11, wherein;

said retirement payload array comprises M rows of memory cells and N of said column structures.

13. The retirement payload array of Claim 12, wherein;

said retirement payload array comprises M read word lines and N read bit lines, further wherein;

each of said N read bit lines is coupled to a corresponding pre-charge device and a corresponding sensing device.

14. The retirement payload array of Claim 13, wherein

said pre-charge devices are pre-charged when said clock signal is in said first or "A" phase.

15. The retirement payload array of Claim 14, wherein;

each of said pre-charge devices is a transistor and each of said sensing devices is a latch.

16. The retirement payload array of Claim 11, wherein;

said gate is a NOR-Gate comprising a first input, a second input and an output, further wherein;

said conditional read circuit comprises:

an inverter, said inverter having an input and an output; and

a NAND-Gate having a first input, a second input, and an output, wherein;

said inverter input is coupled to said clock signal and said inverter output is coupled to said NAND-Gate second input, further wherein;

said NAND-Gate first input is coupled to said advance pointer signal and said NAND-Gate output is coupled to said NOR-Gate first input.

17. The retirement payload array of Claim 16, wherein;

said retirement payload array comprises M rows of memory cells and N of said column structures.

18. The retirement payload array of Claim 17, wherein;

said retirement payload array comprises M read word lines and N read bit lines, further wherein;

each of said N read bit lines is coupled to a corresponding pre-charge device and a corresponding sensing device.

19. The retirement payload array of Claim 18, wherein;

each of said pre-charge devices is a transistor and each of said sensing devices is a latch.

20. The method of Claim 19, wherein;

said retirement payload array is a 192 column, 16-read word line register file structure employing a dynamic, full swing pull down read mechanism.

21. A retirement payload array comprised of modified column structures, each of said modified column structures comprising:

a read bit line;

a pre-charge device coupled to said read bit line, said pre-charge device comprising a transistor;

a sensing device coupled to said read bit line, said sensing device comprising a latch;

at least one memory cell, said memory cell comprising an output coupled to said read bit line and an input;

a NOR-Gate comprising a first input, a second input and an output, said NOR-Gate output being coupled to said input of said at least one memory cell;

a conditional read circuit, said conditional read circuit comprising:

an inverter, said inverter having an input and an output; and

a NAND-Gate having a first input, a second input, and an output, said NAND-Gate output being coupled to

said NOR-Gate first input, said inverter output being coupled to said NAND-Gate second input;

a clock signal, said clock signal having a first or "A" phase and a second or "B" phase, said clock signal being coupled to said input of said inverter of said conditional read circuit, said pre-charge devices being pre-charged when said clock signal is in said first or "A" phase;

an advance pointer signal, said advance pointer signal having a first or inactive phase and a second or active phase, said second or active phase of said advance pointer signal corresponding to a shift in position of a read pointer, said advance pointer signal being coupled to said first input of said NAND-Gate of said conditional read circuit, wherein;

said conditional read circuit initiates a read of said retirement payload array only when, both:

said clock signal is in said "B" phase; and

said advance pointer signal is in said active phase.

22. The retirement payload array of Claim 21, wherein;

said retirement payload array comprises M rows of memory cells and N of said column structures.

23. The retirement payload array of Claim 22, wherein;

said retirement payload array comprises M read word lines and N read bit lines, further wherein;

each of said N read bit lines is coupled to a corresponding pre-charge device and a corresponding sensing device.

24. The method of Claim 21, wherein;

said retirement payload array is a 192 column, 16-read word line register file structure employing a dynamic, full swing pull down read mechanism.